REMARKS/ARGUMENTS

Claims 1, 3-4, 6-8, 10-11, 13-15, 17-18, 20-22 and 24-25 are pending in the present application. Claims 1, 3-4, 8, 10-11, 15, 17-18, 22 and 24-25 were amended; claims 2, 5, 9, 12, 16, 19 and 23 were canceled. No claims were added. Reconsideration of the claims is respectfully requested in view of the above amendments and the following comments.

I. 35 U.S.C. § 101: claims 24-25

The Examiner has rejected claims 24-25 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. This rejection is respectfully traversed.

In rejecting the claims, the Examiner states:

> As per claims 24-25: Claims recite a produce that in carried in a medium included a transmission-type media such digital and analog communication links, wireless communications links, radio frequency, light wave transmissions, etc. The claims fail to meet claimed statutory under 35 U.S.C. 101.

Office Action dated July 13, 2007, page 2.

In response, claims 24 and 25 have been amended to recite a "recordable-type computer readable medium." This terminology is supported on page 64, lines 24-26 of the specification and excludes transmission-type media. Claims 24-25, accordingly, now fully comply with the requirements of 35 U.S.C. § 101 in all respects.

Therefore, the rejection of claims 24-25 under 35 U.S.C. § 101 has been overcome.

II. 35 U.S.C. § 112, claims 4, 11, and 18

The Examiner has rejected claims 4, 11 and 18 under 35 U.S.C. § 112, first and second paragraphs, as being based on a non-enabling disclosure, and as failing to particularly point out and distinctly claim subject matter which applicant regards as the invention. These rejections are respectfully traversed.

In rejecting the claims, the Examiner states:

> Specific critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See In re *Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Claims 4, 11, and 18 recite a second range, and it appears the second range is not the same with the range that is determined in the first time. According to appeal, Applicants show that the specification does not teach second range. These claims that recite the second range fail to be enablement because second range is not included in the disclosure.

> Claims 4, 11, and 18, are indefinite because the claims recite the limitation "second range" that lacks antecedent basis in the specification. To expedite the examination, the interpretation for this limitation is, "within the same contiguous range of instructions".

Office Action dated July 13, 2007, page 3.

Initially, Applicants respectfully submit that the second contiguous range of instructions is fully disclosed in both the specification and in the drawings. For example, on page 61, lines 17-28, reference is made to Figure 31 as illustrating a program 3100 that includes instruction ranges 3102 and 3104 each of which "has been identified as ones of interest for monitoring", and that each range "is used to tell the processor the number of instructions executed in a range, as well as the number of times a range is entered during execution of the program."

Thus, a plurality of contiguous ranges is fully supported by the disclosure. In order to avoid any possible confusion in this regard, claims 4, 11 and 17 have been amended to recite "one contiguous range" and "another contiguous range", and the claims as amended fully satisfy the requirements of 35 U.S.C. § 112, first and second paragraphs, in all respects. Also, it should be noted that the another contiguous range need not be within the same contiguous range as the one contiguous range as interpreted by the Examiner, but may be a separate contiguous range.

Therefore the rejections of claims 4, 11, and 18 under 35 U.S.C. § 112, first and second paragraphs have been overcome.

III. <u>35 U.S.C. § 102, Anticipation: claims 1-25</u>

The Examiner has rejected claims 1-25 under 35 U.S.C. § 102(b) as being anticipated by Intel, "Intel 1A-64 Architecture Software Developer's Manual", Revision 1.1, July 2000, IDS submitted by Applicants, (hereinafter "Intel"). This rejection is respectfully traversed.

In rejecting claims 1, 2 and 5 the Examiner states:

> CLAIM 1: Intel discloses profiling, which has performance counters (p.6-3, sec. 6.1.1.3) used to count occurrence of some events within a specific instruction address range (*'contiguous range of instructions'* (See p. 6-5, sec. 6.1.2: Profiling)). Processor has a program counter that increments every execution (conventional). Intel discloses a method in a data processing system for monitoring execution of instructions. An instruction for execution is identified (See Figure 6-4, p. 6-9, Current Instruction AND Event). It is determined whether the instruction is within a contiguous range of instructions (See Figure 6-4, p. 6-9, Current Instruction AND Event AND Instruction Address: + Check: YES, all of above are true: This explained that when a current instruction is entered for execution, it is checked if it is within a specific addressed range and is an event), and execution information relating to the instruction is generated if the instruction is within the contiguous range of instructions (See Figure 6-4, checked if event monitor is enabled - See Sec. 6.1.3: Event Qualification: See last

bullet: It means that the performance counter counts the event, except situations such as overflow interrupt, pollute, etc.

As per Claim 2: Intel discloses *the generating step comprises: counting each event associated with execution of the instruction if the instruction is within the contiguous range of instructions* (See p. 6-8, second bullet).

As per Claim 5: Intel discloses, *The method of claim 1, wherein the execution information includes at least one of a number of visits to the range of instructions and a number of times the instruction has been executed* (Clearly, whenever the same instruction is passed, the counter is incremented).

Office Action dated July 13, 2007, pages 4 and 5.

Claim 1, as amended herein, is as follows:

1. A method in a data processing system for monitoring execution of instructions, the method comprising:
identifying an instruction for execution;
determining whether the instruction is within a contiguous range of instructions;
responsive to determining that the instruction is within a contiguous range of instructions, counting at least one of a number of times the contiguous range of instructions is entered during execution of a program and a number of times the instruction has been executed; and
providing a result of the counting.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case each and every feature of the presently claimed invention is not identically shown in Intel, arranged as they are in the claims. For example, with respect to claim 1, Intel does not disclose or suggest "responsive to determining that the instruction is within a contiguous range of instructions, counting at least one of a number of times the contiguous range of instructions is entered during execution of a program and a number of times the instruction has been executed."

Intel describes a performance monitoring mechanism in which monitoring can be constrained to a programmable instruction address range. The reference describes, for example, in Section 6.1.3 on page 6-8, that counting of events can be enabled at a level of granularity less than dynamic instruction length of a pipeline which is indicated as being approximately 48 instructions. In Section 6.2.4 on pages 6-18 to 6-

20, Intel describes that the address range selected for checking is controlled by a "tag all" bit, and then describes details of selecting an address range for checking for events.

Intel does not, however, specifically determine whether a particular instruction is within a contiguous range of instructions. At best, Intel selects a subset of a range of instructions, and then monitors all instructions in that subset. Accordingly, Intel does not disclose performing any type of action "responsive to determining that the instruction is within a contiguous range of instructions" as recited in claim 1, and does not anticipate claim 1 for this reason.

Furthermore, Intel does not disclose or suggest performing the specific actions of "counting at least one of a number of times the contiguous range of instructions is entered during execution of a program and a number of times the instruction has been executed" responsive to determining that an instruction is within a contiguous range of instructions as recited in claim 1. In rejecting original dependent claim 5, the Examiner stated "[c]learly, whenever the same instruction is passed, the counter is incremented." Applicants respectfully disagree. Intel nowhere discloses or suggests counting a number of times a contiguous range of instructions is entered during execution of a program or a number of times an instruction [that has been determined to be within a contiguous range of instructions] has been executed.

Events that are monitored in Intel include event rates such as average retired instruction-per-clock cycle data and instruction cache miss rates, and program cycle breakdowns (see for example, Section 6.1.1 on page 6-2). Nowhere does Intel disclose counting at least one of a number of times a contiguous range of instructions is entered during execution of a program and a number of times an instruction determined to be within a contiguous range of instructions has been executed. Therefore, Intel does not disclose "responsive to determining that the instruction is within a contiguous range of instructions, counting at least one of a number of times the contiguous range of instructions is entered during execution of a program and a number of times the instruction has been executed" and does not anticipate claim 1 for this reason as well.

For at least all the above reasons, claim 1 as amended herein is not anticipated by Intel and patentably distinguishes over Intel in its present form.

Independent claims 15 and 24 recite similar subject matter as claim 1 and are also not anticipated by Intel for similar reasons as discussed above with respect to claim 1.

Claims 3, 4, 6 and 7 depend from and further restrict claim 1, and claims 17, 18, 20 and 21 depend from and further restrict claim 15. These claims are also not anticipated by Intel, at least by virtue of their dependency. Furthermore, many of these claims recite additional features that are not disclosed by Intel. For example, claim 4 recites determining whether an instruction is within another contiguous range of instructions, and "responsive to determining that the instruction is within the another contiguous range

of instructions, counting at least one of a number of times the another contiguous range of instructions is entered during execution of the program and a number of times the instruction has been executed."

As indicated above, Intel does not disclose counting a number of times a contiguous range of instructions is entered during execution of a program or a number of times an instruction determined to be within a contiguous range of instructions has been executed, and certainly does not disclose performing such counting with respect to another contiguous range of instructions. Accordingly, claim 4 and corresponding claim 18 patentably distinguish over Intel in their own right as well as by virtue of their dependency.

Independent claim 8 is as follows:

> 8. A method in a data processing system for monitoring access to data in memory locations, the method comprising:
> identifying an access to data in a memory location;
> determining whether the memory location is within a contiguous range of memory locations;
> responsive to determining that the memory location is within a contiguous range of memory locations, counting at least one of a number of times the contiguous range of memory locations is accessed during execution of a program and a number of times the memory location has been accessed; and
> providing a result of the counting.

For similar reasons as discussed above with respect to claim 1, Intel does not disclose or in any way suggest "responsive to determining that the memory location is within a contiguous range of memory locations, counting at least one of a number of times the contiguous range of memory locations is accessed during execution of a program and a number of times the memory location has been accessed" as recited in claim 8.

Claim 8, accordingly and corresponding claims 22 and 25 are not anticipated by Intel and patentably distinguish over Intel in their present form.

Claims 10, 11, 13 and 14 depend from claim 8 and also patentably distinguish over Intel in their present form.

Therefore, the rejection of claims 1-25 under 35 U.S.C. § 102(b) has been overcome.

IV. Conclusion

It is respectfully urged that the subject application is patentable over Intel and that the application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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